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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SANTIAGO, MARICELI	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,723	OH ET AL.	
	Examiner	Art Unit	
	Mariceli Santiago	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,13,14 and 20-23* is/are rejected.

7)☒ Claim(s) *6-10 and 15-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "the channel" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. (US 6,420,726).

Regarding claim 21, Choi discloses a field emission display, comprising a first substrate (11), at least one gate electrode (13) formed in a predetermined gate electrode pattern on the first substrate, a plurality of cathode electrodes (12) formed on the first substrate in a predetermined pattern, at least one first insulation layer (17) formed between the at least one gate electrode and the plurality of cathode electrodes, emitters (15) electrically contacting the cathode electrodes, a second substrate (20) opposing the first substrate with a predetermined

gap therebetween, the first substrate and the second substrate forming a vacuum container, at least one anode electrode (14) formed in a predetermined anode electrode pattern on a surface of the second substrate opposing the first substrate, wherein portions of the cathode electrodes (14) are removed to form emitter-receiving sections (Fig. 4A), one of the emitters (15) being provided in each of the emitter-receiving sections electrically contacting the cathode electrodes, wherein a pixel region is formed at each intersection of a cathode electrode and a gate electrode when the anode electrode is a common anode electrode, or a cathode electrode and an anode electrode when the gate electrode is a common gate electrode, and wherein predetermined voltages are applied to the at least one anode electrode, cathode electrodes and the at least one gate electrode generating an electric field between respective gate electrodes and the emitters such that electrons emitted from emitters are induced toward and strike the second substrate in a corresponding pixel region to realize predetermined images.

Choi fails to explicitly teach the provision of phosphor layers formed in a predetermined phosphor layer pattern on the anode electrode, wherein a pixel region is formed between an emitter and a respective phosphor layer of the predetermined phosphor layer pattern. Choi discloses the use of the field emission display as a flat display panel. It notoriously known to be provide with phosphor patterns on the anode substrate in order to obtain the multi-colored image display flat panels, with pixel regions formed between an emitter and a respective phosphor layer of the predetermined phosphor layer pattern. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate phosphor layers within the flat panel display of Choi in order to obtain the multi-colored image display flat panels.

Regarding claims 22 and 23, Choi discloses a field emission display wherein the at least one gate electrode formed in a predetermined gate electrode pattern is a plurality of gate

electrodes formed in a striped pattern and the at least one anode electrode formed in a predetermined anode electrode pattern is one anode electrode functioning as the common electrode, alternatively, wherein the at least one anode electrode formed in a predetermined anode electrode pattern is a plurality of anode electrodes formed in a striped pattern and the at least one gate electrode formed in a predetermined gate electrode pattern is one gate functioning as the common electrode (Column 2, lines 14-17).

Claims 1-5, 11-14 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kane et al. (US 5,191,217) in view of Choi et al. (US 6,420,726).

Regarding claim 1, Kane discloses a field emission display (Fig. 1), comprising a first substrate (101), at least one gate electrode (103) formed in a predetermined pattern on the first substrate, a plurality of cathode electrodes (108) formed on the first substrate in a predetermined pattern, at least one emitter (107), at least one first insulation layer formed between the at least one gate electrode (103) and the plurality of cathode electrodes (108), at least one second insulation layer (104) being formed on the cathode electrode, at least one focusing electrode (105) formed on the second insulation layer, a second substrate (106) provided opposing the first substrate with a predetermined gap therebetween, the first and second substrates forming a vacuum assembly when interconnected, at least one anode electrode (106) formed on the second substrate opposing the first substrate.

Kane is silent in regards to the limitations of the at least one emitter being mounted within an opening of the cathode electrode. However, in the same field of endeavor, Choi discloses a field emission display wherein the electron emission sources (15) can be locally formed around at least one hole pierced in the cathodes (12) at the intersections with the gates (13), or anodes, the electron emission sources (15) can be formed at any positions on the

cathodes at the intersections with the gates, moreover, the formation of the electron emission sources (15) on the edge of the cathodes has an advantage in that the strongest field is experimentally formed at the edge thereof. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the electron emitter structure disclosed by Choi in the field emission display of Kane in order to provide a formation of the electron emission sources (15) on the edge of the cathodes having an advantage in that the strongest field is experimentally formed at the edge thereof.

Moreover, in an alternative embodiment, Choi discloses providing the gate electrode, formed in a predetermined pattern, on the substrate, providing a first insulation layer over the gate electrodes and providing a plurality of cathode electrodes, formed in a predetermined pattern, over the first insulation layer, in order to easily form electron emission materials serving as electron emission sources on the cathodes, also, emitted current can be controlled with low voltage by field emission at the edge of cathodes, and the uniformity of emitted current can be improved by the formation of various patterns. Furthermore, the gate electrodes are formed below an insulation layer formed below the cathodes, so that, if an appropriate amount of voltage is applied to the gate electrodes, an electrical field caused by the gate voltage transmits the insulation layer, and thus a strong electrical field is formed in electron emission sources. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the gate, insulation layer and cathode arrangement disclosed by Choi in the field emission display of Kane in order to easily form electron emission materials serving as electron emission sources on the cathodes, also, emitted current can be controlled with low voltage by field emission at the edge of cathodes, and the uniformity of emitted current can be improved by the formation of various patterns.

The combination Kane-Choi fail to explicitly teach the provision of phosphor layers formed in a predetermined phosphor layer pattern on the anode electrode, wherein a pixel region is formed between an emitter and a respective phosphor layer of the predetermined phosphor layer pattern. Kane and Choi disclose the use of the field emission display as a flat display panel. It notoriously known to be provide with phosphor patterns on the anode substrate in order to obtain the multi-colored image display flat panels, with pixel regions formed between an emitter and a respective phosphor layer of the predetermined phosphor layer pattern. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate phosphor layers within the flat panel display of Kane-Choi in order to obtain the multi-colored image display flat panels.

Regarding claim 2, the combination Kane-Choi discloses a field emission display wherein the cathode electrodes and the gate electrodes are crossed in a stripped pattern (Choi, Figs. 4A-4D). The same reasons for combining stated in the rejection of claim 1 applies.

Regarding claim 3, the combination Kane-Choi discloses a field emission display wherein the cathode electrodes and the anode electrodes are crossed in a stripped pattern. The same reasons for combining stated in the rejection of claim 1 applies.

Regarding claim 4, Kane discloses a field emission display wherein the second insulation layer has a channel (opening within the second insulation layer) formed corresponding to the emitter, the second insulation layer being formed on the cathode electrode such that the emitter is positioned within the channel.

Regarding claim 5, Kane fails to disclose the limitation of the emitter being formed as longitudinal single structure with long ends in a direction along which the gate electrode is patterned. However, Choi discloses a field emission display wherein the number of circular or different-shaped field emission material figures is controlled to obtain the maximum uniform

electron emission effect at the minimum power, according to all of the conditions such as the standards such as the gap between cathodes, the gap between a cathode and a gate, and the gap between a cathode and an anode, the material of an insulation layer, and a voltage applied to each electrode. Accordingly, it would have been obvious to one having ordinary skill in the art to provide a emitter being formed as longitudinal single structure with long ends in a direction along which the gate electrode is patterned, since such modification involves a change in shape that is within the applied teaching, as evidenced by Choi, in order to obtain the maximum uniform electron emission effect at the minimum power.

Regarding claim 11, Kane fails to disclose the limitation wherein the emitter includes carbon nanotubes. However, Choi discloses a field emitter display comprising an emitter which includes carbon nanotubes for their low voltage operation requirements. It has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Thus, it would have been obvious to one having ordinary skills in the art at the time the invention was made to have the emitter including carbon nanotubes, since the selection of known materials for a known purpose is within the skill of the art.

Regarding claim 12, Kane discloses a field display device wherein the emitter is divided into a plurality of sections for each pixel.

Regarding claim 13, Kane discloses a field emission display (Figs. 4A-4D), comprising a first substrate, a gate electrodes formed in a predetermined pattern on the first substrate, a plurality of cathode electrodes formed on the first substrate in a predetermined pattern, the cathode electrodes forming intersection regions with the gate electrodes corresponding to pixel regions, at least one first insulation layer between the at least one gate electrode and the plurality of cathode electrodes, an emitter, a second insulation layer having a plurality of

channels formed corresponding to the emitters, the second insulation layer being formed on the cathode electrodes such that the emitters are positioned within the channels, focusing electrodes formed on the second insulation layer, a second substrate provided opposing the first substrate with a predetermined gap wherebetween, the first and second substrate forming a vacuum assembly when interconnected, an anode electrode formed on at least one side of the second substrate opposing the first substrate. Kane is silent in regards to the limitations of the emitter being mounted within an opening of the cathode electrodes and phosphor layers formed on the at least one anode electrode in a pattern corresponding to positions of the emitter.

In the same field of endeavor, Choi discloses a field emission display comprising a plurality of gate electrodes, formed in a predetermined pattern, on the substrate, providing a first insulation layer over the gate electrodes and providing a plurality of cathode electrodes, formed in a predetermined pattern, over the first insulation layer. Furthermore, Choi discloses a field emission display wherein the electron emission sources (15) can be locally formed around at least one hole pierced in the cathodes (12) at the intersections with the gates (13), or anodes, the electron emission sources (15) can be formed at any positions on the cathodes at the intersections with the gates, moreover, the formation of the electron emission sources (15) on the edge of the cathodes has an advantage in that the strongest field is experimentally formed at the edge thereof. The disclosed arrangement easily form electron emission materials serving as electron emission sources on the cathodes, furthermore, emitted current can be controlled with low voltage by field emission at the edge of cathodes, and the uniformity of emitted current can be improved by the formation of various patterns. Furthermore, the gate electrodes are formed below an insulation layer formed below the cathodes, so that, if an appropriate amount of voltage is applied to the gate electrodes, an electrical field caused by the gate voltage transmits the insulation layer, and thus a strong electrical field is formed in electron emission

sources. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the gate, insulation layer and cathode arrangement disclosed by Choi in the field emission display of Kane in order to easily form electron emission materials serving as electron emission sources on the cathodes, also, emitted current can be controlled with low voltage by field emission at the edge of cathodes, and the uniformity of emitted current can be improved by the formation of various patterns.

The combination Kane-Choi fail to explicitly teach the provision of phosphor layers formed in a predetermined phosphor layer pattern on the anode electrode. Kane and Choi disclose the use of the field emission display as a flat display panel. It notoriously known to be provide with phosphor patterns on the anode substrate in order to obtain the multi-colored image display flat panels. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate phosphor layers within the flat panel display of Kane-Choi in order to obtain the multi-colored image display flat panels.

Regarding claim 14, Kane fails to disclose the limitation of the emitter being formed as a longitudinal single structure with long ends in a direction along which the gate electrode is patterned. However, Choi discloses a field emission display wherein the number of circular or different-shaped field emission material figures is controlled to obtain the maximum uniform electron emission effect at the minimum power, according to all of the conditions such as the standards such as the gap between cathodes, the gap between a cathode and a gate, and the gap between a cathode and an anode, the material of an insulation layer, and a voltage applied to each electrode. Accordingly, it would have been obvious to one having ordinary skill in the art to provide a emitter being formed as longitudinal single structure with long ends in a direction along which the gate electrode is patterned, since such modification involves a change in shape

that is within the applied teaching, as evidenced by Choi, in order to obtain the maximum uniform electron emission effect at the minimum power.

Regarding claim 20, Kane fails to disclose the limitation wherein the emitter includes carbon nanotubes. However, Choi discloses a field emitter display comprising an emitter which includes carbon nanotubes for their low voltage operation requirements. It has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Thus, it would have been obvious to one having ordinary skills in the art at the time the invention was made to have the emitter including carbon nanotubes, since the selection of known materials for a known purpose is within the skill of the art.

Regarding claim 21, Kane discloses a field emission display (Fig. 1), comprising a first substrate (101), at least one gate electrode (103) formed in a predetermined gate electrode pattern on the first substrate, a plurality of cathode electrodes (108) formed on the first substrate in a predetermined pattern, at least one first insulation layer (102) formed between the at least one gate electrode and the plurality of cathode electrodes, emitters (107) electrically contacting the cathode electrodes, a second substrate (106) opposing the first substrate with a predetermined gap therebetween, the first substrate and the second substrate forming a vacuum container, at least one anode electrode (106) formed in a predetermined anode electrode pattern on a surface of the second substrate opposing the first substrate, and wherein predetermined voltages are applied to the at least one anode electrode, cathode electrodes and the at least one gate electrode generating an electric field between respective gate electrodes and the emitters such that electrons emitted from emitters are induced toward and strike the second substrate in a corresponding pixel region to realize predetermined images.

Kane fails to disclose the limitations of phosphor layers formed in a predetermined phosphor layer pattern on the anode electrode, wherein portions of the cathode electrodes are removed to form emitter-receiving sections, one of the emitters being provided in each of the emitter-receiving sections electrically contacting the cathode electrodes, wherein a pixel region is formed between an emitter and a respective phosphor layer of the predetermined phosphor layer pattern at each intersection of a cathode electrode and a gate electrode when the anode electrode is a common anode electrode, or a cathode electrode and an anode electrode when the gate electrode is a common gate electrode. However, in the same field of endeavor Choi discloses a field emission display comprising a plurality of gate electrodes, formed in a predetermined pattern, on the substrate, providing a first insulation layer over the gate electrodes and providing a plurality of cathode electrodes, formed in a predetermined pattern, over the first insulation layer, and phosphor layers formed on the at least one anode electrode in a pattern corresponding to positions of the emitter, wherein a pixel region is formed at each intersection of a cathode electrode and a gate electrode when the anode electrode is a common anode electrode, or a cathode electrode and an anode electrode when the gate electrode is a common gate electrode. Furthermore, Choi discloses a field emission display (Figs. 4A-4D) wherein the electron emission sources (15) can be locally formed around at least one hole pierced in the cathodes (12) at the intersections with the gates (13), or anodes, the electron emission sources (15) can be formed at any positions on the cathodes at the intersections with the gates, moreover, the formation of the electron emission sources (15) on the edge of the cathodes has an advantage in that the strongest field is experimentally formed at the edge thereof. The disclosed arrangement easily form electron emission materials serving as electron emission sources on the cathodes, furthermore, emitted current can be controlled with low voltage by field emission at the edge of cathodes, and the uniformity of emitted current can be

improved by the formation of various patterns. Furthermore, the gate electrodes are formed below an insulation layer formed below the cathodes, so that, if an appropriate amount of voltage is applied to the gate electrodes, an electrical field caused by the gate voltage transmits the insulation layer, and thus a strong electrical field is formed in electron emission sources. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the gate, insulation layer and cathode arrangement disclosed by Choi in the field emission display of Kane in order to easily form electron emission materials serving as electron emission sources on the cathodes, also, emitted current can be controlled with low voltage by field emission at the edge of cathodes, and the uniformity of emitted current can be improved by the formation of various patterns.

The combination Kane-Choi fail to explicitly teach the provision of phosphor layers formed in a predetermined phosphor layer pattern on the anode electrode, wherein a pixel region is formed between an emitter and a respective phosphor layer of the predetermined phosphor layer pattern. Kane and Choi disclose the use of the field emission display as a flat display panel. It notoriously known to be provide with phosphor patterns on the anode substrate in order to obtain the multi-colored image display flat panels, with pixel regions formed between an emitter and a respective phosphor layer of the predetermined phosphor layer pattern. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate phosphor layers within the flat panel display of Kane-Choi in order to obtain the multi-colored image display flat panels.

Regarding claims 22 and 23, the combination Kane-Choi disclose a field emission display wherein the at least one gate electrode formed in a predetermined gate electrode pattern is a plurality of gate electrodes formed in a striped pattern and the at least one anode electrode formed in a predetermined anode electrode pattern is one anode electrode functioning

as the common electrode, alternatively, wherein the at least one anode electrode formed in a predetermined anode electrode pattern is a plurality of anode electrodes formed in a striped pattern and the at least one gate electrode formed in a predetermined gate electrode pattern is one gate functioning as the common electrode (Choi, Column 2, lines 14-17). The same reasons for combining stated in the rejection of claim 21 applies.

Allowable Subject Matter

Claims 6-10 and 15-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 6, the references of the Prior Art of record fails to teach or suggest the combination of the limitations as set forth in claim 6, and specifically comprising the limitation of a channel is formed by a stepped portion of the second insulation layer.

Regarding claims 7-9, claims 7-9 are allowable for the reasons given in claim 6 because of their dependency status from claim 6.

Regarding claims 10 and 19, the references of the Prior Art of record fails to teach or suggest the combination of the limitations as set forth in claims 10 and 19, and specifically comprising the limitation the second insulation layer is opaque.

Regarding claim 15, the references of the Prior Art of record fails to teach or suggest the combination of the limitations as set forth in claim 15, and specifically comprising the limitation of the channels are formed by a stepped portion of the second insulation layer.

Regarding claims 16-18, claims 16-18 are allowable for the reasons given in claim 15 because of their dependency status from claim 15.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (571) 272-2464. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11/22/05

Mariceli Santiago
Primary Examiner
Art Unit 2879